NICMAR University, Pune

Position: Vice-Chancellor

Name: Shriram Divakar Markande
Email: sdmarkande@gmail.com
Mobile: 9422517315
Gender: Male
Date of Birth: 06-Mar-1964

Education Detail

Education Level	Board / University	Institute / School / College	Marks	CGPA	Year
PhD	Bharathi Vidyapeeth Deemed University	BVCOE	0.00	0.00	2010
Subjects / Specialization: Electronics Engineering					
Post Graduation	Pune University	COEP	66.21	0.00	2000
Subjects / Specialization: Electrical- Control Systems					
Graduation	Shivaji University	Walchand College of Engineering, Sangli	58.82	0.00	1985
Subjects / Specialization: Electrical- Specialization Electronics					

Work Experience (Total: 14Y 6M)

#	Organization	Designation	From	To	Duration
1	Bharati Vidyapeeth	HOD, Lecturer	Jul 1987	Feb 2002	14Y 6M

Research Publication

#	Title	Journal	Year
1	Reinforcement Learning Algorithm for Improving Spectral Energy Efficiency Using Large Intelligent Surfaces	International Journal of Communication Systems	Jun-2025
2	Efficient Design of Up Sampler and Down using Single Electron Transistor-Metal Oxide Semiconductor Field Effect Transistor	Journal of VLSI Circuits and Systems	Jul-2025
3	Mathematical Modeling and Synthesis of Reversible Cryptographic Logic	The Journal of Dynamics And Control	Sep-2025
4	Efficient Design of Reversible Adder and Multiplier Using Peres Gates	Applied Sciences	Jan-2024
5	An Evaluation of the Signal to Noise Ratio (SNR) of Next Generation Wireless Communication Systems using Large Intelligent Surfaces: Deep Learning Approach	International Journal of Electrical and Electronics Research (IJEER)	Nov-2023
6	Intelligent Beyond 5G Systems: Upcoming Wireless Communication Systems	Lecture Notes in ElectricalEngineering	Jan-2022
7	Improving the Performance and Satisfaction of Students in Embedded Systems with PBL Approach	International Journal on Recent and Innovation Trends in Computing and Communication	Jul-2020
8	Performance Optimization of Polar Code Based OFDM Volte System Using Taguchi Method	International Journal of Advanced Science and Technology(IJAST)	Sep-2020
9	Performance Evaluation of AODV and DSR Protocols in Different Environments of WSN	International Journal of Electronics Engineering Research (IJEER)	Apr-2012
10	Cartesian Coordinate System based Dynamic Location Management Scheme	International Journal of Electronic Engineering Research (IJEER)	Jan-2009
11	Microcontroller Based Temperature Controller - Implementation of Fuzzy Logic	Computer Engineering Journal of the Institution of Engineers (India)	May-2004

Administrative Experience (Total: 0Y 0M)

#	Post	Institution	From	To	Duration

Statutory Authorities

#	Institution	Statutory Forum	From	To
1	Savitribai Phule Pune University	Member, Senate	Aug 2010	Jul 2011

PhD Student Guided

#	Guide No	Co-Guide No
1	2	-